fore also the rate R for the light. Because of carrier transport across the junction, it is not valid to say that $-dn/dt = n/\tau_n$. Nevertheless, (3) is correct, as one can see by inspection since each side of the equality is clearly equal to the total number of carriers which recombine per second.

$$\frac{-d}{dt}(t_n p + t_p n) = t_n \frac{p}{\tau_p} + t_p \frac{n}{\tau_n}; \quad (3)$$

Using (2) to eliminate p from (3), and then solving for $R = -n^{-1} dn/dt$ yields

$$R = 1/\tau = \omega(1/\tau_p) + (1-\omega)1/\tau_n \quad (4)$$

where

$$\omega = [1 + (n_0/p_0)(t_p/t_n)]^{-1}.$$

For high injection rate the doping is neglected. Mathematically speaking, this is equivalent to repeating the above derivation with n_0 and p_0 interpreted as injected carrier densities. From (2) and charge neutrality it follows that $n = p = n_0 = p_0$, and ω is reduced to $(1 + t_p/t_n)^{-1}$. Thus the light decay rate given by Eq. (4) is equal to the average of minority-carrier rates weighted by the junction displacement distance. Experimentally, in our devices, $\tau_n \leqslant 4$ ns for $p \approx (2\text{–}5) \times 10^{17}$ cm^{-3} and $\tau_p \geqslant 30$ ns for $n \approx (1\text{–}2) \times 10^{17}$ cm^{-3} as shown in Figs. 1 and 2. In order to understand why the power decreases with the lifetime, the radiative efficiency of the p-type InGaAsP must be assumed lower than that of the n-type material. Otherwise the power output of a LED would stay constant regardless of the lifetime changes. This would result in a changing power-bandwidth product, in contradiction with previous models[2] and our experimental results. Thus, a gradual shift of the p-n junction position within the active layer, and the corresponding gradual change from hole to electron injection are consistent with decreasing power output and increasing LED speed.

In summary we have prepared double heterostructure wafers of InGaAsP/InP in which the p-n junction position is moved across the active layer. As the InGaAsP active layer is converted to p type by solid state diffusion of Zn during crystal growth, the LED's become faster and their power output decreases. Thus rise time in excess of 30 ns and optical power launched into fiber of $\sim 150\,\mu$W are observed for devices with an n-type active layer. For the entirely p-type active layer devices t_r is reduced to ~ 4 ns and the launched power decreases to $\sim 50\,\mu$W. These results are attributed to p-n junction displacement resulting in a gradual shift of minority carriers from holes to electrons.

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Orientation selection by zone-melting silicon films through planar constrictions

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Recrystallization of encapsulated Si films on SiO_2 by zone-melting produces films composed of several grains approximately 1 mm wide and extending the length of the scan. Within grains there are sub-boundaries. We report a technique for producing recrystallized Si films of a single orientation. The technique consists of patterning polysilicon with a narrow, planar constriction and passing a molten zone through it so that only one orientation propagates beyond the constriction. We also show that sub-boundaries can be eliminated in the constriction.

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Previous papers have described the crystallographic and electrical properties of Si films produced by zone-melting recrystallization using a movable graphite strip heater oven.[1–7] Typically, these films consist of several distinct grains about 1 mm wide that extend the length of the region scanned. Grains with (100) texture and ⟨100⟩ directions within 20 degrees of the scan direction tend to predominate by occluding grains of other orientations. Grain boundaries are detrimental to electronic devices because they are electrically charged and present a barrier to carrier conduction. In

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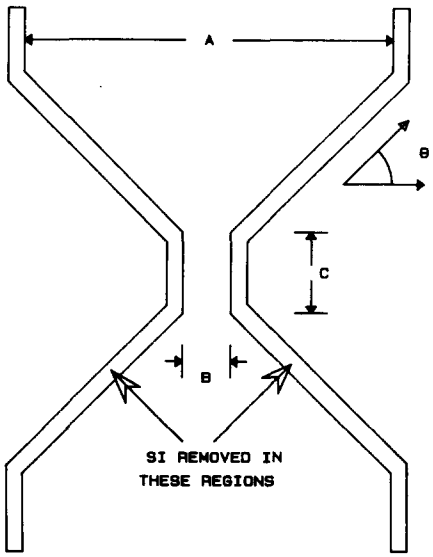

FIG. 1. Variety of hourglass-shaped constriction patterns etched into the poly-Si layers. Parameter A varied from 50–1000 μm, B from 2.5–75 μm, C from 7.5–250 μm, $\theta = 0°$ and 45°.

this letter we report a technique for selecting a single grain orientation by passing the molten zone through a narrow, planar constriction or "neck" patterned into the encapsulated polysilicon film, and show that sub-boundaries can be eliminated in the constriction, under appropriate conditions. These sub-boundaries appear as linear defects within grains as revealed by chemical etching and consist of arrays of dislocations.

Figure 1 illustrates the type of hourglass-shaped patterns we have used for grain selection. To prepare samples, polysilicon films 0.5 μm thick were deposited by chemical vapor deposition (CVD) on 1-μm-thick SiO_2 layers thermally grown on (100) Si substrates. This was followed by deposition of 0.1-μm-thick films of SiO_2 by CVD. The hourglass-shaped pattern was defined in photoresist, transferred to the

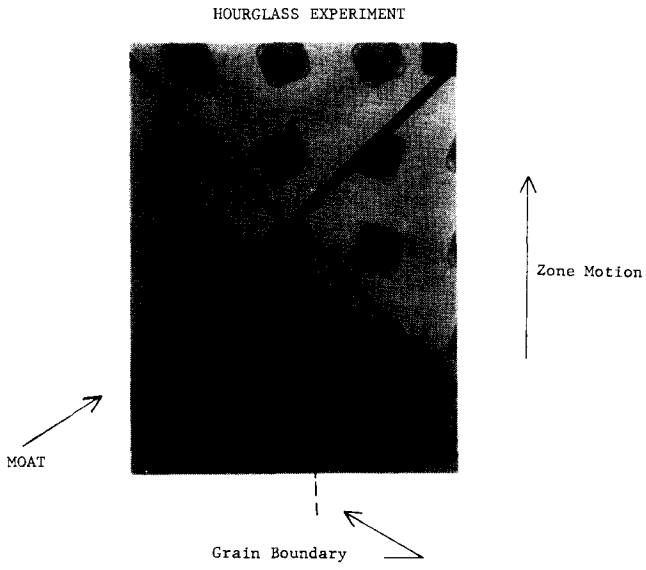

FIG. 2. Selection of a single orientation from two initial grains by zone-melting recrystallization through the neck of an hourglass structure. The etch pits are 50 μm apart.

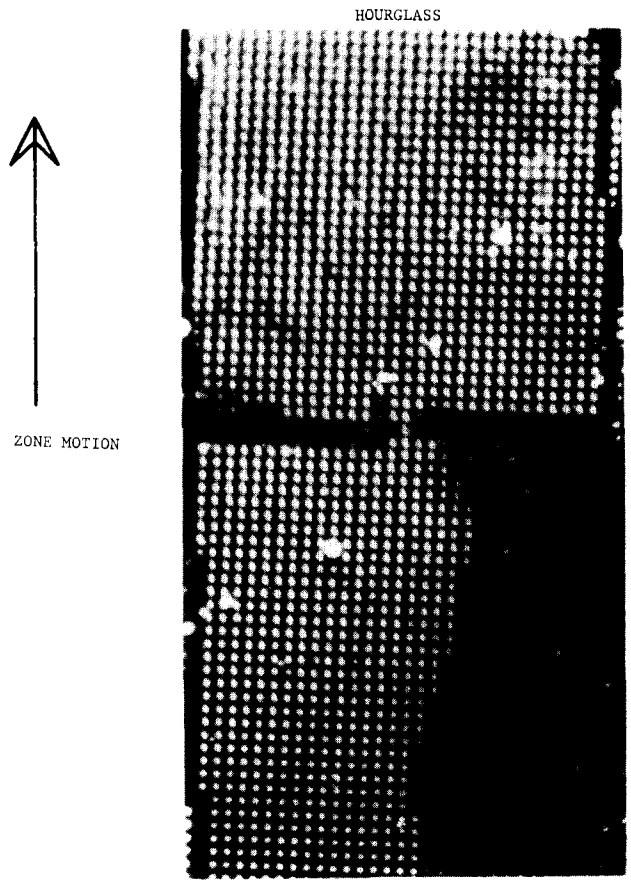

FIG. 3. Large area view of orientation selection illustrated by the oblique illumination of etch pits. Etch pits are 50 μm apart.

CVD SiO_2 by chemical etching, and duplicated in the polysilicon by chemical etching down to the underlying SiO_2. The photoresist was removed and an encapsulation layer of 2 μm SiO_2 and 30 nm Si_3N_4 was deposited over the hourglass structure.

When films prepared in the above manner are recrystallized, a single grain orientation is selected as the solidification front passes through the neck. This is illustrated in Fig.

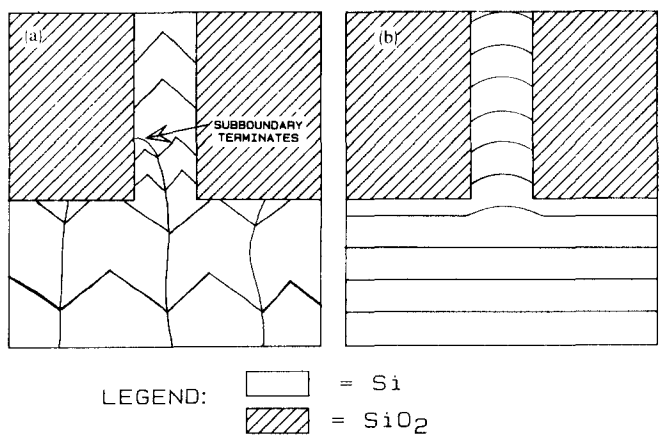

FIG. 4. (a) Schematic depiction of sub-boundary behavior in the neck region. The faceted growth front is sketched at several times during its passage through the neck region. (b) Sketch depicting isothermal contours in the neck region.

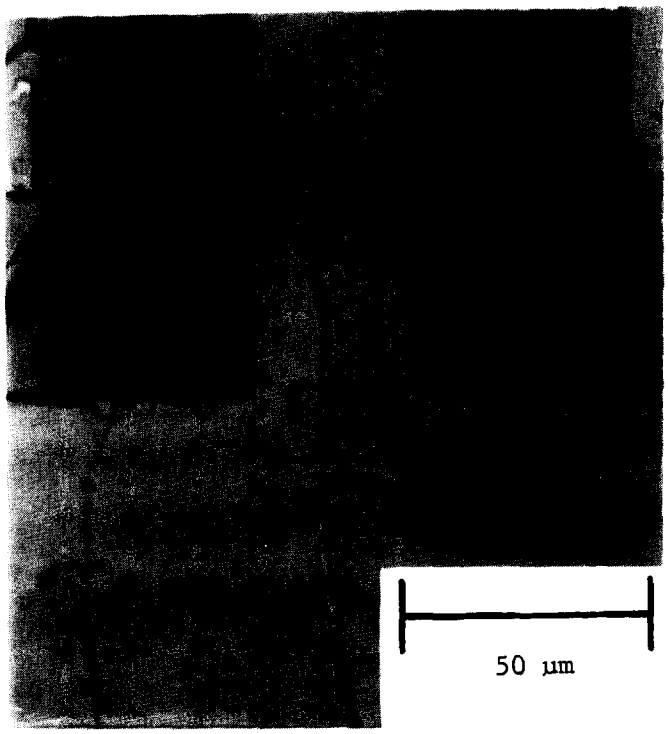

FIG. 5. Optical micrograph showing termination of a sub-boundary in the neck region.

2 in which crystallographic orientation is revealed by an array of pits etched into the film.[8] These pits are inverted, truncated pyramids bounded by (111) facets; the pit diagonals are ⟨100⟩ directions. The (111) facets reflect light specularly and oblique illumination with a collimated light source can reveal the shapes and locations of distinct grains. This is used in Fig. 3 to illustrate grain selection.

The parameters A, B, C, and θ, as defined in Fig. 1, were not critical to grain selection. However, for $\theta = 0$, dendritic growth occurred in the left and right corners of the hourglass structure if the zone scan speed was greater than 1 mm/s. Presumably, the selected orientation could not grow laterally from the neck before the silicon in the corners undercooled sufficiently to induce dendritic growth. If the zone motion speed was reduced to 0.9 mm/s, dendritic growth did not occur. In no case did hourglass structures with $\theta = 45°$ exhibit dendritic growth or yield other than a single orientation.

Biegelsen *et al.*[9,10] have also described the patterning of polysilicon films prior to recrystallization and have also used constrictions. However, their objective was not to select a grain orientation, but to control thermal profiles and provide for expansion at solidification.

In addition to grain selection, sub-boundary elimination occurred in the neck region of the hourglass structure if the neck width was approximately equal to the average distance between sub-boundaries. This average distance depends on scan speed and Si film thickness.[2] Sub-boundaries reappeared beyond the neck region when the pattern widened to about 100 μm. These results are shown schematically in Fig. 4 and experimentally in Fig. 5.

Sub-boundaries occur in silicon at the interior corners of a faceted solid-liquid interface where two (111) planes meet at an angle.[1,2] Since the angle between facets is fixed, the width of a chevron-shaped pair of facets is proportional to the distance a chevron protrudes into the liquid silicon. Sub-boundary elimination in the neck region indicates that the faceting of the solid-liquid interface is modified in the neck region so that only a single chevron passes through. We believe that this modification occurs because the Si in the middle of the neck is cooler than at the edges, leading to concave isothermal contours. This in turn would tend to enlarge the facets, align the chevron with the middle of the neck, and thereby drive sub-boundaries and grain boundaries toward the edges of the neck.[11]

In conclusion, a method for selecting a single grain orientation during zone melting of encapsulated silicon on insulator has been developed. The method is simple since it relies on etching a photolithographically defined pattern into the Si film. In addition, sub-boundary elimination may be accomplished in Si stripes of width approximately equal to or slightly larger than the averge distance between sub-boundaries.

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